REMARKS

Claims 1, 8 and 11 were rejected under 35 U.S.C. 112, second paragraph, as being incomplete or omitting essential structural cooperative relationships of elements. Specifically, the Examiner points to the packet replicator and the replicating packet step. Applicant proposes amendments to claims 1, 8 and 11 to address this issue noted by the Examiner. Specifically, Applicant has amended claims 1, 8 and 11 to emphasize the use of destination pointers which are disclosed in the specification as supporting packet replication (such as would occur when two different destination pointers point at the same slot so as to replicate output of the same packet to two different destinations; see, Figure 3). Withdrawal of the Section 112 rejection is requested.

Claims 1-14 and 32-35 were rejected under 35 U.S.C. 103(a) as being unpatentable over Chapman in view of Barnes and Wegner. Claims 15-23 and 26-38 were rejected under 35 U.S.C. 103(a) as being unpatentable over Chapman in view of Barnes.

Claim 1 has been amended to recite "storage means for holding packets of the input packet streams at ***arbitrarily addressable*** locations each identifiable by an address." The Examiner has previously pointed to Chapman's input buffer 320/324 which is a FIFO queue for temporary packet storage (see, col. 7, line 51). While the Chapman FIFO buffer may have an address, it is clear that the data stored therein is not arbitrarily addressable. Applicant's disclosed embodiment for the storage means is an SRAM which has plurality of arbitrarily addressable storage locations. This feature of arbitrarily addressable storage locations is not taught by Chapman's FIFO buffer.

Claim 1 has further been amended to recite "a ***packet allocation table*** comprising an array including a plurality of ***slots holding*** for each new incoming packet a ***source identifier*** identifying the source of the packet and the ***arbitrary address*** in the storage means where the packet is held, the packet allocation table further including a ***plurality of destination pointers***, each destination pointer associated with one of the output ports, ***each destination pointer being assignable to any slot*** so as to identify the output ports associated with the intended destinations of a held packet, the ***assigning of each destination pointer to a slot being derived using the assignment data structure***." In this context, the "assignment data structure" identifies "***for each source*** of the input packet stream ***at least one destination*** to which each input packet stream is to be routed." Thus, the source of the packet is linked by the assignment data structure to one or more destinations, and the packet allocation table provides a slot for each packet which contains source identification information with the assignment data structure driving assignment

of the plurality of the destination pointers to slots in the packet allocation table to select packets for output, those packets being retrieved from storage in memory at the arbitrary address which is also provided in the slot. Applicant asserts that this structure and operation is neither taught nor suggested by the cited prior art.

Applicant previously claimed a "packet allocation data structure." The new limitation of "a packet allocation data table" with "a plurality of slots" and "a plurality of destination pointers assignable to any slot" more clearly claims the present invention and distinguishes the claimed invention over the routing table disclosed by Chapman.

In Chapman, an incoming packet is received and stored in a FIFO queue (the input buffer) until a decision can be made as handling. Logic is invoked to determine which "class" the packet belongs and to which output port of the switch the packet is to be routed. The output port determination is made by Chapman's logic using a routing table that ***maps a destination address of the packet to an output port***. The destination address used in the mapping operation is contained in the header of the received packet.

The Chapman routing table does not include a "plurality of destination pointers [wherein] each destination pointer [is] assignable to any slot." In this context, each slot "hold[s] for each new incoming packet a ***source identifier identifying the origin of the packet*** and the arbitrary address in the storage means where the packet is held." The Chapman routing table simply maps a packet ***destination address*** to an output port, and thus any destination pointing operation in Chapman is based on this destination address-output port mapping information. The claimed invention is different because each destination pointer points at any slot, and each slot contains packet ***source information*** and stored packet address information, and routing based on destination pointing is performed through a source-driven assignment. Chapman does not route on the claimed basis.

The Examiner has cited to Gaudet in support of a position taken that it is well known to have a packet allocation data structure based on source identifier and address where a packet is stored. Applicant has amended the claims to specifically recite a table format including slots wherein each slot contains the source information and storage address. As discussed above, this is not taught by Chapman. Applicant further submits that this is not taught by Gaudet. The Examiner points to Gaudet col. 7, lines 28-38. This section of Gaudet teaches that it is known in the art to segregate incoming packets based on source ID. The memory is loaded in order with sequential cells originating from a same source. This allows a single frame of data to be stored

in contiguous memory locations. This teaching from Gaudet, however, does not reach the amended claim language relating to a packet allocation table, slots and each slot including source information and memory address information.

The Examiner has further cited to Wegner which teaches a queuing mechanism that ensures that all ports are available before allowing a broadcast delivery. While this technique would facilitate a broadcast operation, the Wegner teachings do not address the deficiencies of Chapman with respect to amended claim 1. Wegner fails to teach the claimed "packet allocation data table" with "a plurality of slots" and "a plurality of destination pointers assignable to any slot."

Claim 1 is accordingly patentable over the cited prior art.

Claim 8 has been amended like claim 1, and Applicant asserts that claim 8 is patentable over the cited prior art for at least the same reasons as claim 1.

Claim 11 is a method claim which has been amended to claim method steps which distinguish over the cited prior art for at least the same reasons as claim 1.

Claim 15 has also been amended to distinguish over the cited prior art. Amended claim 15 includes limitations similar to those presented above with respect to claim 1, and is asserted to be patentable over the cited prior art for at least the same reasons as claim 1.

Claim 36 has been amended to clarify the claim language. Applicant respectfully traverses the rejection and requests reconsideration.

Claim 36 recites "a source-to-destination matrix mapping each source of the input packet streams coupled to the input ports to one or more destinations, for packets within those input packet streams, which are coupled to receive the output packet streams from the output ports." The Examiner asserts that this limitation is met by a routing table in Chapman. However, the Chapman routing table maps ***destination address*** to output by reading the destination address from a header of the packet. The claimed invention maps ***source*** of the packets to output destination.

The Examiner cites to Chapman col. 10, lines 5-12 and asserts that this has a teaching for "holding the source address." Applicant disagrees. There is no mention of source address at the cited location. Nonetheless, any mention of source address in Chapman is not relevant because it is clear that Chapman routes based on destination address to output mapping. There is no teaching in Chapman for the claimed "a source-to-destination matrix mapping each source of the input packet streams … to one or more destinations."

Claim 36 further recites "a packet allocation table which includes a plurality of slot locations, each slot location storing a source identifier which identifies a source of the received packet stream to which a given packet belongs linked in the slot of the packet allocation table to an address in the memory for the addressable memory location where that given packet has been stored by the processor." The distinctions between Applicant's "packet allocation table" and Chapman's routing table have been discussed in detail above with respect to claim 1. Applicant reiterates that Chapman fails to teach or suggest the claimed packet allocation table.

Claim 36 has further been amended to recite "a destination pointer, associated with each one of the output ports, implemented by the processor for pointing to a slot location in the packet allocation table from which the address of the given packet is retrieved, ***the destination pointer pointing to the slot location when the source identifier in the slot is associated with a source that is mapped through the source-to-destination matrix to a destination coupled to an output port and that output port is associated with that destination pointer***." Then highlighted portion emphasizes a difference in operation of the claimed invention over the prior art. This language is intended to claim the operations illustrated in Applicant's Figures 2 and 3. The destination pointer points to a slot in Figure 3 if that slot contains a source identification which can be mapped through Figure 2 to a destination wherein that destination is associated with an output port (see Figure 1) that is associated with that destination pointer. This structural and operational relationship is neither disclosed nor suggest by the cited prior art.

The Examiner has previously pointed to the Chapman routing table and asserted that a memory address or memory pointer must be present. While this may be true, it is not relevant to the invention as claimed. The destination pointer and source-to-destination matrix information, along with the slot information in the allocation table, are all interrelated in the claimed invention and this interrelationship is not taught by Chapman and a basic memory address pointer operation.

Applicant respectfully submits that all claims of the application are in condition for favorable action and allowance.

Dated: July 22, 2009

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